Lead-Lag Compensators for Higher Order SISO Dead-Time System: Time Domain Approach

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A simplified algorithm for designing a lead-lag compensator in time domain is proposed in this paper. The lead-lag compensator is designed in order to satisfy the control specifications in time domain such as damping ratio, maximum overshoot settling time and steady sate error. Using the correlation between frequency and time domain, the algorithm can also be used to solve the required compensator in the case the design specifications are given in time domain, such as phase margin and gain margin. The other finding of this research is a new Proportional Derivative (PD) compensator that is obtained after an artistic modification of the designed lead-lag compensator, herein called fortunate compensator. The proposed algorithm make it possible and easily handle the design of PI, PD and PID controller that satisfy time response or frequency response specifications. This work was supported by Basic Science Research Program through the NRF funded by the Ministry of Education, Science and Technology (2012012532). This work was also supported by Priority Research Centers Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2014R1A6A1031189).