Fabrication of Backside-Illuminated CMOS Image Sensor Using 3-D Interconnect Technologies

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In a complementary metal oxide semiconductor (CMOS) image sensor, a light receiving element, a digital control block, and a peripheral circuit such as an analog-to-digital converter are arranged at a limited area within a chip. Thus, an area ratio of a pixel array per a chip area is limited to about 40%. Furthermore, a pixel size is greatly reduced for implementation of high quality images. Accordingly, an amount of light that one light receiving element can collect is reduced and noise is increased, causing various problems such as image loss. Complex 3-D integration structures have many technologically relevant applications such as decreasing optical crosstalk in CMOS image sensor. The dense vertical interconnection of multiple circuit layers have been developed using a three-dimensional(3D) circuit integration technology including wafer bonding, wafer thinning, deep Si etching process. We demonstrate thatprocess integration of a back-illuminated 2 mega pixel CMOS sensor utilizing 3D integration and wafer manufacturing operations with SOI epi wafer. The 3D integration processes were evaluated to get stable performance of backside illuminated CMOS image sensor.